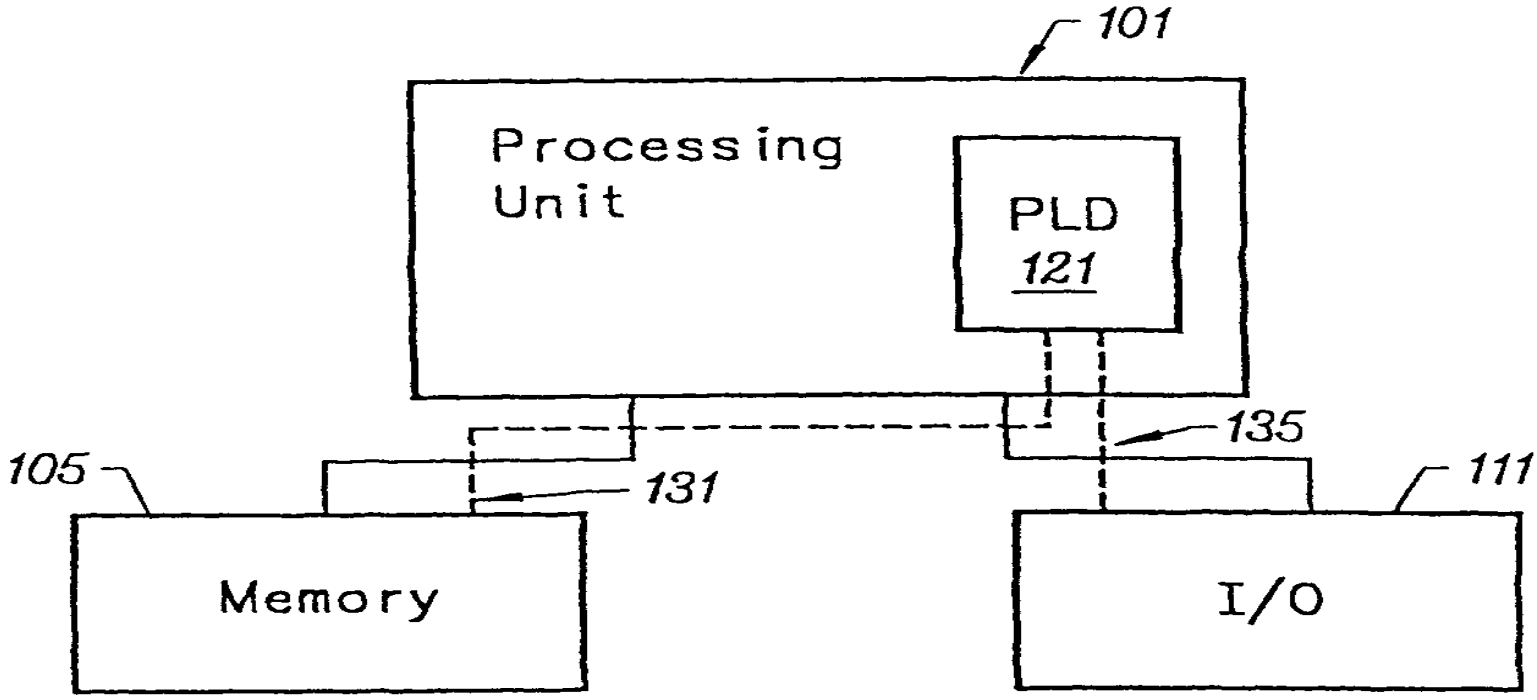
101
Processing Unit
PLD
121
135
105
131
111
Memory
I/O

FIG. 1

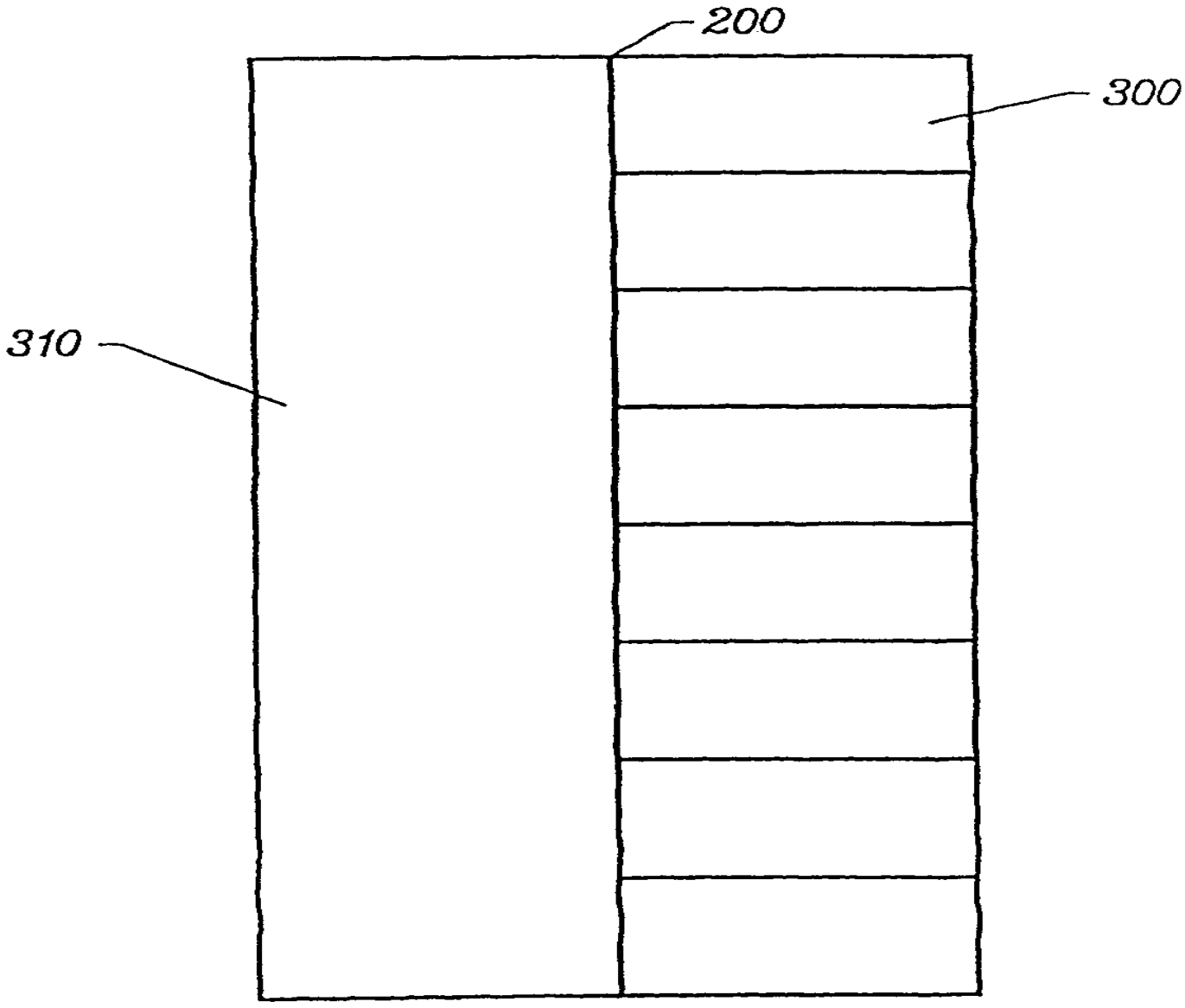
200
300
310

FIG. 3

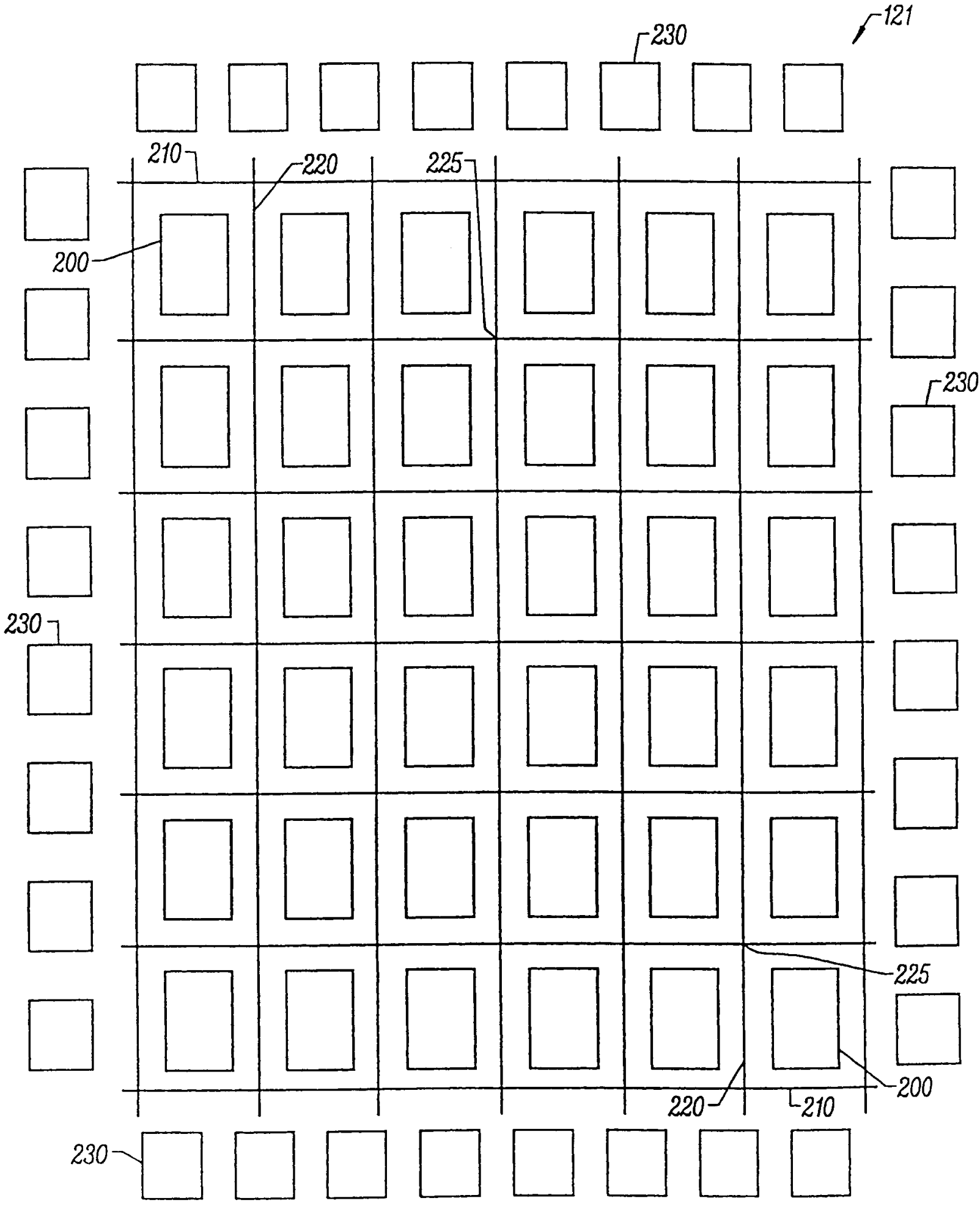

FIG. 2

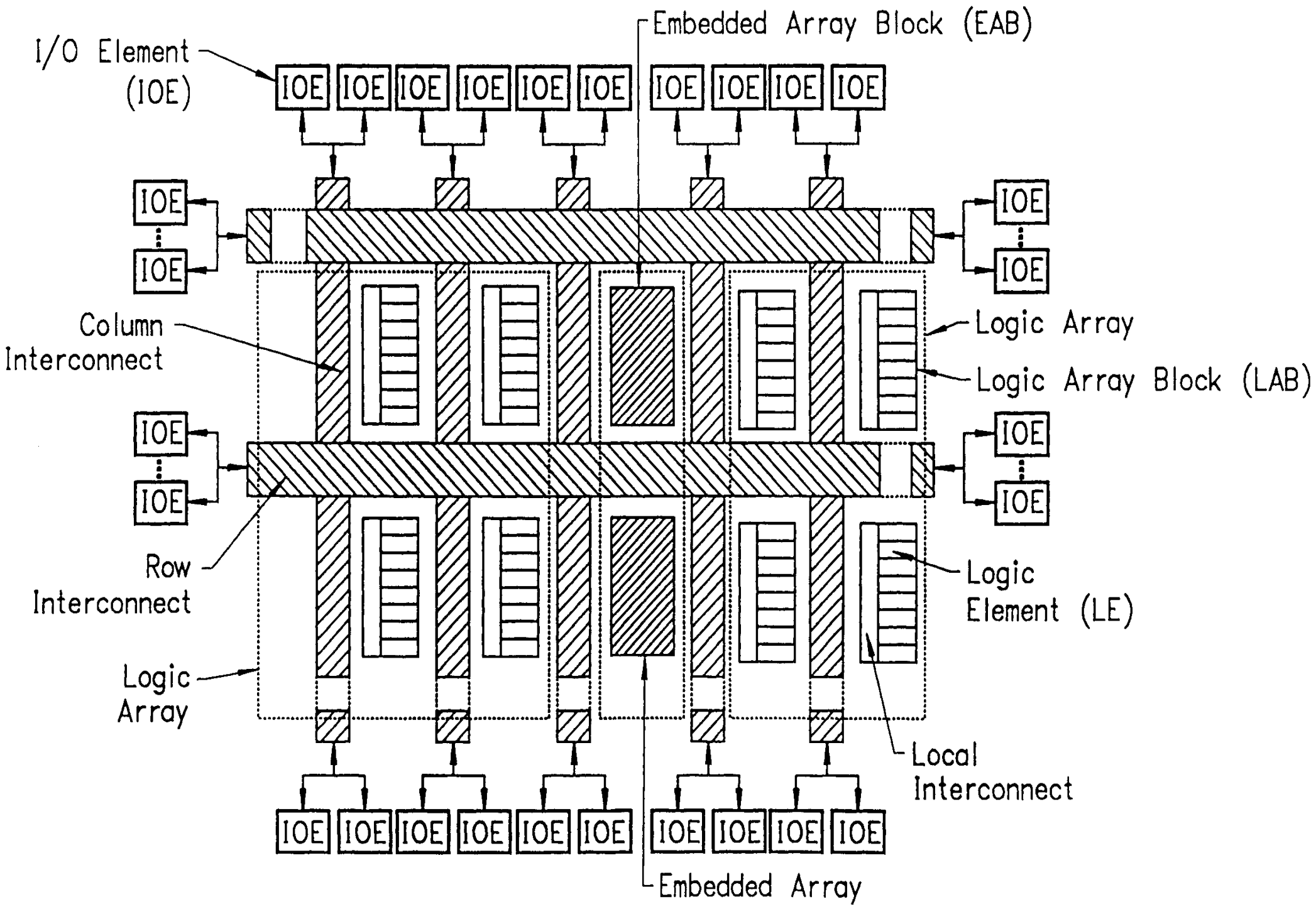
I/O Element (IOE)
Embedded Array Block (EAB)
IOE
Column Interconnect
Logic Array
Logic Array Block (LAB)
Row Interconnect
Logic Element (LE)
Logic Array
Local Interconnect
Embedded Array

FIG. 4

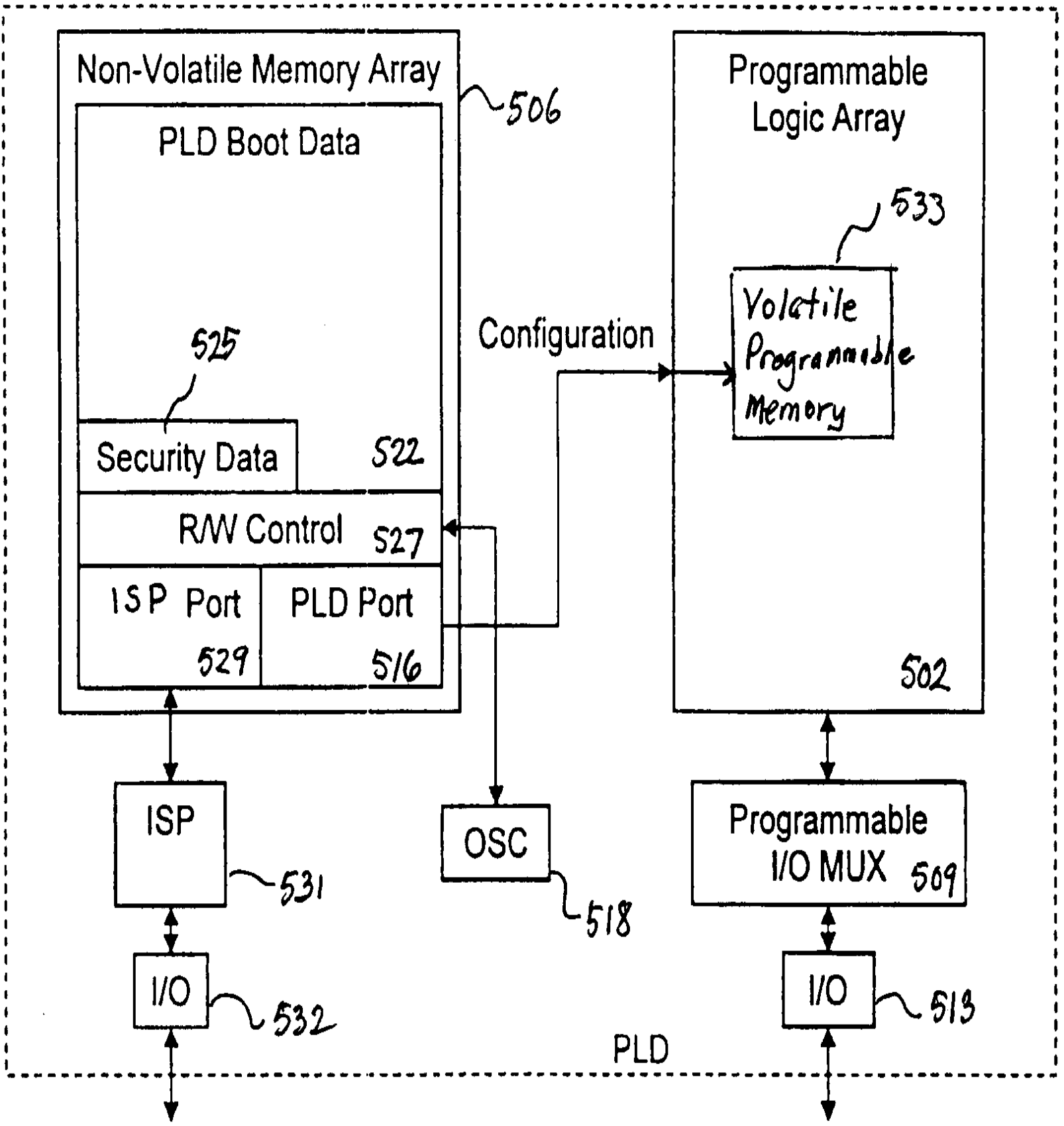
Non-Volatile Memory Array
506
PLD Boot Data
525
Security Data
522
R/W Control
527
ISP Port
529
PLD Port
516
Configuration
Programmable Logic Array
533
Volatile Programmable Memory
502
ISP
531
OSC
518
Programmable I/O MUX
509
I/O
532
I/O
513
PLD

FIGURE 5

Inhibiting Chip Operation Pending Successful Memory Read

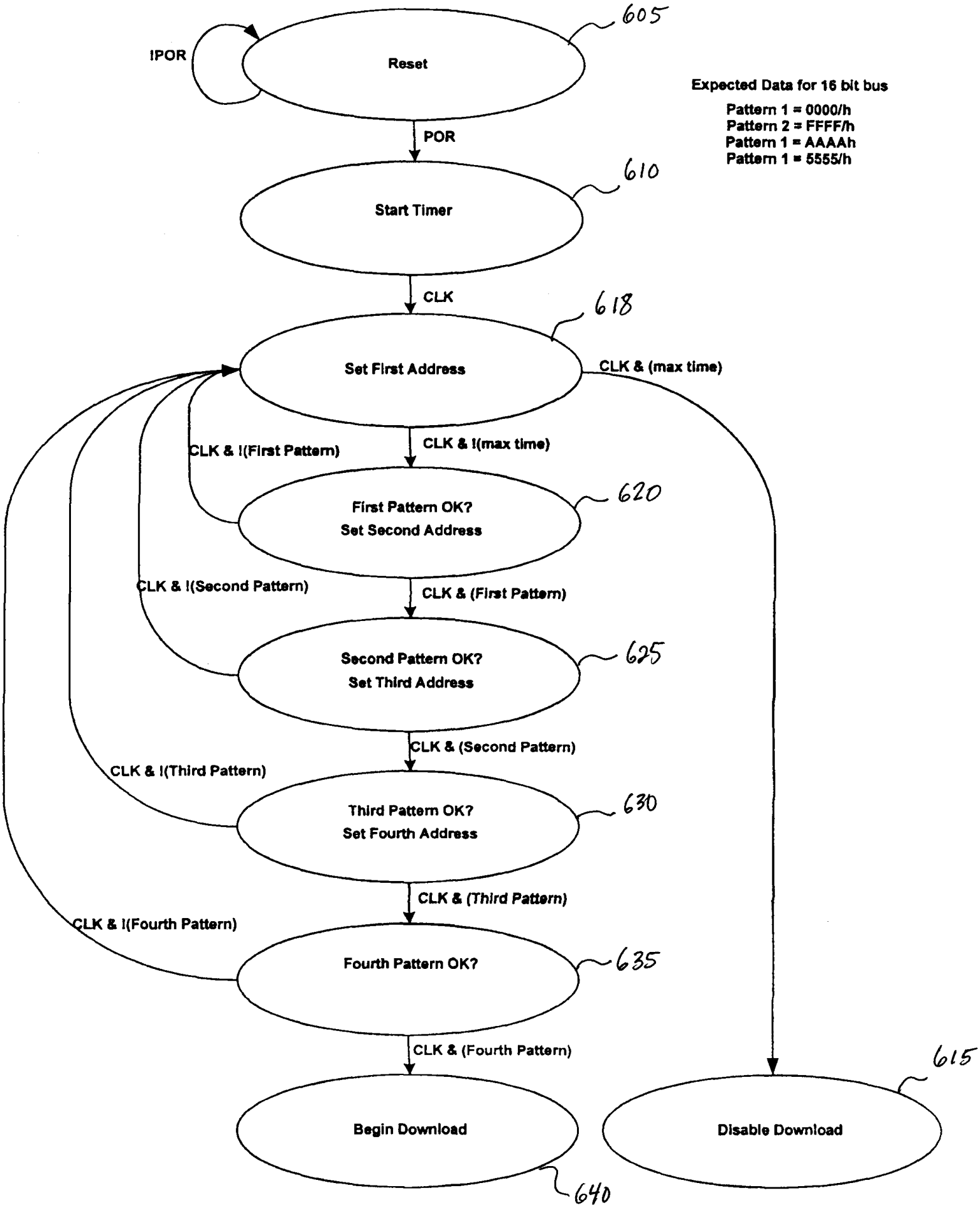

FIGURE 6

Low Voltage Read Verification Methodology

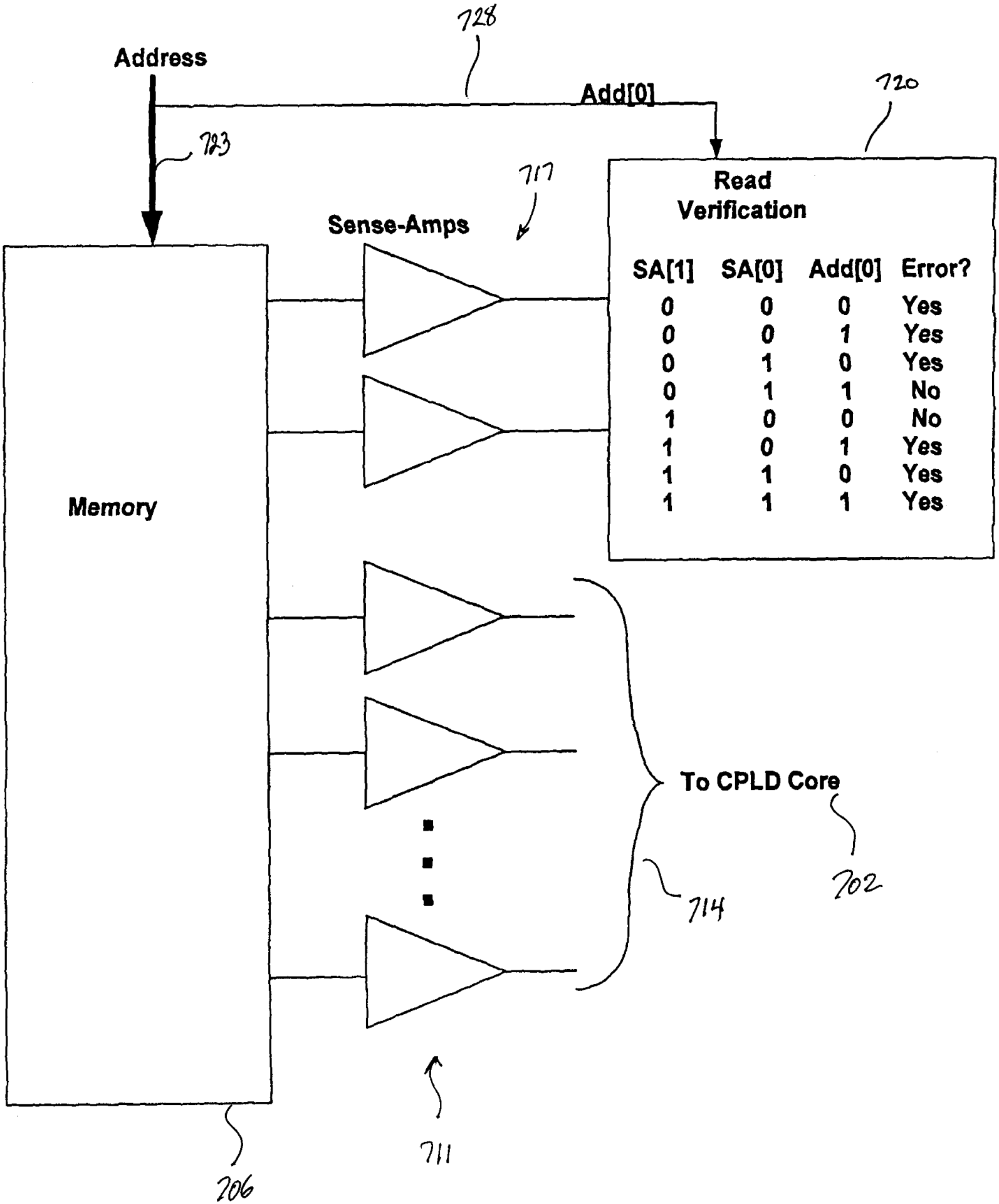

FIGURE 7